REMARKS

Applicant thanks the Examiner for acknowledging receipt of Applicant's foreign priority documents that have been submitted pursuant to 35 U.S.C. §119. Applicant respectfully requests reconsideration of the prior art rejections that have been set forth by the Examiner under 35 U.S.C. §§102 and 103.

By this amendment, Applicant has modified independent claims 1 and 3 to more specifically underscore the distinctions between the claimed invention and the prior art. Applicant respectfully submits that the prior art of record, whether considered alone, or in combination, fail to either teach or suggest Applicant's invention as now claimed. Applicant's claimed invention is directed to an improved semiconductor imaging housing or structure wherein pairs of positioning holes and attaching holes are located on opposed sides of the housing structure such that a line connecting the positioning holes and a line connecting the attaching holes intersects substantially in the central portion of the chip member. Furthermore, the line connecting the positioning holes as well as the line connecting the attaching holes is skewed relative to each of the side walls of the housing member.

The prior art of record fails to provide any teaching or suggestion whatsoever regarding this advance in the art. Applicant's claimed structure provides an improved imaging housing which significantly allows a smaller chip housing to be utilized due to the strategic placement of the respective positioning and attaching holes. The primary reference upon which the Examiner relies in rejecting the claims, the *Arai* United States Patent No. 5,686,758 is merely directed to a semiconductor chip package wherein the reference character 52 denotes an attaching hole of the semiconductor device and the reference character 53 denotes a position hole of the device.

As shown in Figure 1, a line drawn between the attaching holes 52 and this prior art reference is substantially perpendicular to the side walls of the package housing illustrated

therein. The same holds true for the remaining illustrations in this prior art reference. See, for example, Figure 4, wherein the line drawn between the holes in the central portion bisects the chip centrally. Applicant's claimed invention is directed to a chip structure wherein lines drawn between both the positioning and the attaching holes are each respectively skewed with respect to each of the side walls in the overall package. This advantageously provides improved positioning and securing of the chip housing member.

Furthermore, with regard to claim 5, Applicant submits that the *Arai* reference fails to provide any teaching or suggestion whatsoever regarding the transparent member for sealing of the semiconductor element and there is no disclosure whatsoever regarding a structure wherein the surface of the package is made to be higher than a top surface of the transparent member as claimed.

Accordingly, in light of the foregoing, Applicant respectfully submits that all claims now stand in condition for allowance.

Respectfully submitted,

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CLEAN VERSION OF CLAIMS

1. A package for containing semiconductor element comprising:

a housing having a recess portion for containing a semiconductor element; and

a pair of positioning holes and a pair of attaching holes respectively provided at opposed side portions of said housing,

wherein a line between said pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the side walls of the housing and the line between the attaching holes is skewed with respect to each of the side walls.

3. A semiconductor device comprising:

a semiconductor element;

a housing having a recess portion for containing said semiconductor element; and

a pair of positioning holes and a pair of attaching holes respectively provided at opposed side portions of said housing;

wherein a line between the pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of the side walls of the housing and the line between the attaching holes is skewed with respect to each of the side walls.

5. A semiconductor device comprising:

a semiconductor element;

a housing having a recess portion for containing said semiconductor element;

a pair of attaching holes provided at opposed side portions of said housing at a surface of said package; and

a transparent member for sealing said semiconductor element in said recess portion;

wherein said surface of said housing is made to be higher than a top surface of said transparent member.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail on February 3, 2003 in an envelope addressed to:

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